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Allwood, Shari, J., Allwood & Associates, Inc., Meeting Planning Services

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Shari J. Allwood
Vice President
Allwood & Associates, Inc., Meeting Planning Services
8279 Midland Road
Mentor, OH 44060

8. PERFORMING ORGANIZATION REPORT NUMBER

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Air Force Office of Scientific Research
4015 Wilson Blvd., Room 732
Arlington, VA 22203-1977
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14. ABSTRACT

Please reference attached Final Program/Abstract Book for review of abstracts of presentations from the Workshop.

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15. SUBJECT TERMS
Substrate-induced effects, etching, implantation, plasma processing, interface defects, ohmic contacts, process-induced traps, thermal and electronic stress.

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U			UU		Shari J. Allwood 440/951-1380

Steven Binari
Naval Research Laboratory
Code 6852
Washington, DC 20375
USA
Phone: (202) 404-4616
Fax: (202) 767-0455
E-mail: binari@nrl.navy.mil

Katherine Bogart
Sandia National Laboratories
Org 1126, MS 0601
PO Box 5800
Albuquerque, NM 87185
USA
Phone: (505) 844-6323
Fax: (505) 844-3211
E-mail: khbogar@sandia.gov

Karim Boutros
Rockwell Scientific Center
Materials and Devices
1049 Camino Dos Rios
Thousand Oaks, CA 91360
USA
Phone: (805) 373-4104
Fax: (805) 373-4860
E-mail: kboutros@rwsc.com

Leonard Brillson
The Ohio State University
205 Dreese Laboratory
2015 Neil Avenue
Columbus, OH 43210
USA
Phone: (614) 292-8015
Fax: (614) 688-4688
E-mail: brillson.1@osu.edu

W.J. Choyke
University of Pittsburgh
Physics and Astronomy
Pittsburgh, PA 15260
USA
Phone: (412) 624-9251
Fax: (412) 624-1479
E-mail: choyke+@pitt.edu

James Cooper (presented via phone)
Purdue University
School of Electrical and Computer Engineering
465 Northwestern Avenue
West Lafayette, IN 47907-2035
USA
Phone: (765) 494-3514
Fax: (765) 494-2706
E-mail: cooperj@ecn.purdue.edu

Robert Davis
North Carolina State University
Box 7907
Raleigh, NC 27695-7907
USA
Phone: (919) 515-3272
Fax: (919) 515-7724
E-mail: robert_davis@ncsu.edu

Alan Doolittle
Georgia Institute of Technology
School of Electrical Engineering
777 Atlantic Drive
Atlanta, GA 30332-0250
USA
Phone: (404) 894-9884
Fax: (404) 385-0343
E-mail: alan.doolittle@ece.gatech.edu

Zhaoqiang Fang
Wright State University
Semiconductor Research Center/Physics Dept.
3640 Colonel Glenn Highway
Dayton, OH 45435
USA
Phone: (937) 775-3525
Fax: (937) 775-2222
E-mail: zhaoqiang.fang@wright.edu

Leonard Feldman
Vanderbilt University
Physics and Astronomy
Stevenson Center
Nashville, TN 27235
USA
Phone: (615) 343-7273
Fax: (615) 343-1708
E-mail: Leonard.c.feldman@vanderbilt.edu

Paul Fini
University of California, Santa Barbara
Bldg. 503, Room 1355
Santa Barbara, CA 93106-5050
USA
Phone: 805/893-2573
Fax: 805/893-8170
E-mail: fini@engineering.ucsb.edu

Robert Fitch
AFLR/SNDD
Bldg. 620, Rm S2-W66
2241 Avionics Circle
Wright-Patterson AFB, OH 45433-7322
USA
Phone: (937) 255-1874 x 3453
Fax: (937) 255-2306
E-mail: robert.fitch@wpafb.af.mil

Remis Gaska (presented via phone)
Sensor Electronic Technology, Inc.
1195 Atlas Road
Columbia, SC 29209
USA
Phone: (803) 647-9757
Fax: (803) 647-9770
E-mail: Gaska@s-et.com

David Gotthold
EMCORE
145 Belmont Drive
Somerset, NJ 08873
USA
Phone: (732) 271-9090, ext. 4279
Fax: (732) 271-9686
E-mail: David_Gotthold@emcore.com

Evelyn Hu
University of California at Santa Barbara
Department of Materials
Electrical and Computer Engineering
Santa Barbara, CA 93106-9560
USA
Phone: (805) 893-2368
Fax: (805) 893-8170
E-mail: hu@ece.ucsb.edu

Gregg Jessen
Air Force Research Laboratory
AFRL/SND, Building 620
2241 Avionics Circle
Wright-Patterson AFB, OH 45433-7322
USA
Phone: (937) 255-1874, ext. 3384
Fax: (937) 255-8656
E-mail: Gregg.Jessen@wpafb.af.mil

Dan Johnstone
Virginia Commonwealth University
Electrical Engineering
601 West Main Street
Richmond, VA 23284
USA
Phone: (804) 827-7000, ext. 357
Fax: (804) 828-4269
E-mail: DJohnstone@vcu.edu

Ken Jones
U.S. Army Research Laboratory
2800 Powder Mill Road
Adelphi, MD 20783-1197
USA
Phone: (301) 394-2005
Fax: (301) 394-4562
E-mail: kajones@arl.army.mil

Asif Khan (presented via phone)
University of South Carolina
Room 3A79
Swearingen Buliding
Columbia, SC 29208
USA
Phone: (803) 777-7941
Fax: (803) 777-2447
E-mail: asif@engr.sc.edu

William Lampert
US Army Research Office
PO Box 12211
Research Triangle Park, NC 27709-2211
Phone: 919/549-4325
Fax: 919/549-4399
E-mail: lampertwv@aro.arl.army.mil

Umesh Mishra
University of California at Santa Barbara
Department of ECE
Room 5107
Santa Barbara, CA 93106
USA
Phone: (805) 893-8956
Fax: (805) 893-8714
E-mail: mishra@ece.ucsb.edu

William Mitchel
Air Force Research Laboratory
AFRL/MLPS
3005 Hobson Way, Room 243
Wright-Patterson AFB, OH 45433-7707
USA
Phone: (937) 255-4474, ext. 3214
Fax: (937) 255-4913
E-mail: william.mitchel@wpafb.af.mil

Suzanne Mohney
Penn State
Materials Science and Engineering
109 Steidle Building
University Park, PA 18602
USA
Phone: (814) 863-0744
Fax: (814) 865-2917
E-mail: mohney@ems.psu.edu

Robert Nemanich
North Carolina State University
Department of Physics
110 Cox Hall
Raleigh, NC 27695
USA
Phone: (919) 515-3225
Fax: (919) 515-7331
E-mail: robert_nemanich@ncsu.edu

Robert Okojie
NASA-Glenn Research Center
Sensors and Electronics Technology
21000 Brookpark Road
Cleveland, OH 44136
USA
Phone: (216) 433-6522
Fax: (216) 433-8643
E-mail: robert.okojie@grc.nasa.gov

Pirouz Pirouz
Case Western Reserve University
Dept. of Materials Science and Engineering
1900 Euclid Ave., 510 White Building
Cleveland, OH 44106-7204
USA
Phone: (216) 368-6486
Fax: (216) 368-3209
E-mail: pxp7@cwru.edu

Mulpuri Rao
George Mason University
Electrical and Computer Engineering
4400 University Drive, MSN:1G5
Fairfax, VA 22030-4444
USA
Phone: (703) 993-1612
Fax: (703) 993-1601
E-mail: rmulpuri@gmu.edu

Deepak Selvanathan
University of Illinois
319 Micro & Nanothechnology Laboratory
208 North Wright Street
Urbana, IL 61801
USA
Phone: (217) 333-4052
Fax: (217) 244-6375
E-mail: Selvanat@uiuc.edu

Brian Skromme
Arizona State University
Department of Electrical Engineering
Box 875706
Tempe, AZ 85287-5706
USA
Phone: (408) 965-8592
Fax: (408) 965-8118
E-mail: skromme@asu.edu

Jim Speck
University of California at Santa Barbara
Materials Department
Santa Barbara, CA 93106
USA
Phone: (805) 893-8005
Fax: (805) 893-8983
E-mail: speck@mrl.ucsb.edu

Mike Spencer
Cornell University
Electrical and Computer Engineering
Rm 418, Phillips Hall
Ithaca, NY 14853
USA
Phone: (607) 255-6271
Fax: (607) 255-4742
E-mail: spencer@ee.cornell.edu

Gerald Witt
Air Force Office of Scientific Research
AFOSR/NE
4015 Wilson Blvd., Room 713
Arlington, VA 22203-1954
USA
Phone: (703) 696-8571
Fax: (703) 696-8481
E-mail: gerald.witt@afosr.af.mil

Scott Wolter
US Army Research Office
PO Box 12211
Research Triangle Park, NC 27709-2211
Phone: 919/549-4353
Fax: 919/549-4399
E-mail: scott.wolter@us.army.mil

Colin Wood
Office of Naval Research
Code 313
800 North Quincy Street
Arlington, VA 22217-5660
USA
Phone: (703) 696-4218
Fax: (703) 696-2611
E-mail: Woodc@onr.navy.mil

Ed Yu
University of California at San Diego
ECE Department
9500 Gilman Drive, MC0407
LaJolla, CA 92093-0407
USA
Phone: (858) 534-6619
Fax: (858) 822-3425
E-mail: ety@ece.ucsd.edu

Mary Ellen Zvanut
University of Alabama at Birmingham
Physics Department
1530 3rd Avenue South, CH 310
Birmingham, AL 35244-1170
USA
Phone: (205) 934-6661
Fax: (205) 934-8042
E-mail: zvanut@phy.uab.edu

Meeting Planning Services Provided by:
Shari Allwood
Allwood & Associates, Inc.
8279 Midland Road
Mentor, OH 44060
PH: 440/951-1380
Fax: 440/951-1381
E-mail: AllwoodInc@aol.com

Tri-Services Workshop on Process Induced Defects in Wide Bandgap Semiconductors
August 17-21, 2003, The Riverside Inn, Grants Pass, OR – Critique Form Summary

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# of Attendees: 36 (3 presented via phone and were not present)
# of Critique Forms Returned: 26

Three Things I liked most about the Workshop:

- Open forum to discuss good and bad results; good interactions between participants -- good variety of topics and areas; relaxed atmosphere – short session blocks.
- Diverse topics (material, devices, physics, etc.); meeting/talking with all the participants.
- The update on results and hypotheses/conclusions regarding these results; the chance to discuss ideas, concepts and future research; the chance to establish interactions.
- Opportunity to discuss common interests; good discussions/interaction; great jetboat ride!
- Opportunity for formal and informal discussion; scene setters were excellent; excursion, breaks were excellent.
- Technical interactions off-line; excellent discussion.
- Informality; super organization; cool lecture hall.
- Generally, the right people were here; excellent discussions; good overall coverage of workshop sub-topics; scene-setters were good, also.
- Location; topic, extensive discussions.
- Talks; outings; format/interaction.
- High-quality technical presentations; good opportunities for social interactions.
- High-quality presentations and discussions; interesting location; well focused.
- Exchange of research ideas; collaboration opportunities.
- Opportunities to interact; activities designed to develop collaborations; organization and structure.
- Informality; opportunity to discuss about collaborations; evening activities.
- The choice of speakers invited to this workshop and the topics in discussion; the efforts by the organizing committee to have a great workshop; the location and excursion trips.
- Opportunity to interact (talk) about potential collaborations; opportunity to speak with tri-service funding folks; openness of speakers.
- Good interaction between fundamental and device researchers; good place for meeting; good support from Shari.
- Range of subjects: from devices to basic defects; breadth of techniques; atmosphere – encouraging discussion/recreation.
- Excellent talks; good location.
- Quality of presentations; focused manner of the workshop; planning.
- Format; open discussion; topic importance/focus.
- Tone: the concept of sharing info/establishing collaborations was done well, and I think it worked; Godo group of people present – good spread and overlap of interest; good to keep the group together with meals and activities.
- Interaction; information (talks); surroundings.
- "Down" time (outings); balance of discussion time with presentations.
- Open communication; desire to collaborate.

Three areas in which the Workshop might be improved:

(Note: Many of the "phone" oriented comments are related to three presentations made via phone. Between Friday evening and Sunday evening, five cancellations were received, four of whom were speakers. Three forwarded their PowerPoint presentations and presented their work via phone. This will NOT be offered in the future, and was provided as an effort to not lose 20% of the scheduled presentations.)

- Stop the phone-ins!
- Keep track of the no-shows; tell the speakers how long to speak for – don't set the number of viewgraphs.
- Organization of how presentations are done (standard format and/or centralized computer for PowerPoint presentations.)
- No more phone presentations – maybe one day video teleconferencing will be the norm, but personal interactions are optimum.
- Figure out how to keep participants for full length; have welcoming reception later – check with attendee arrival times.
- Increase the number of "industry" participants.
- Include more theory (even though little is available); tutorial on device goals would be helpful; discussion on DoD needs applications would be helpful.
- Phone talks.
- Subtopic discussions were not carried sufficiently to get to conclusions (Where are we now? What do we do next?)
- Linking materials and devices further – this may be more of a suggestion for a conference topic.
- Audio conferencing had some value, but eliminated the changes for future questions and interaction; pause for a 20-30 minute Q&A discussion period after a set of papers on the same general theme; The confusion with DARPA and the Martinez e-mail caused people to cancel or make presentations from their home site.
- No phone presentations.
- No external off-site talks.
- Fewer phone-in presentations; longer breaks for discussion in small groups; just a suggestion for the caterer: a tray for dirty dishes after breakfast.
- I agree that the phone-in presentations should not be repeated!
- Talk by phone call should not be encouraged.
- All SiC talks on Wed. – result in GaN community absences; like to see more industry involvement.
- No telephone presentations.
- Longer breaks – maybe suggest informal discussion topics or panel discussion – not real fond of this one; add slide describing areas of interest or willingness to collaborate.
- No more cancellations!
- Avoid phone talks.
- Even better scene-setting – Jim Choyke did a great job – not everyone took these responsibilities fully; more focus on raising challenges, followed by discussion.
- Avoid DARPA involvement; concentrate funding from OXRs and avoid XRL money/fundraising.

Outstanding Speaker Award:

Name	# of Votes
Ed Yu	6
Jim Choyke	4
Bob Nemanich	4
Bob Fitch	2
Alan Doolittle	2
Robert Okojie	1
Brian Skromme	1
Mike Spencer	1
Pirouz Pirouz	1
Bob Davis	1
Len Brillson	1
Jim Speck	1
Mary Ellen Zvanut	1
Karim Boutros	1

Suggestions for future Workshops:

Semiconductor device packaging
Chemistry of III-V nitride growth MBE & OMVPE
Light-emitting structures (III-V, II-VI, Quantum dots, Si, …)
Near-field techniques and their application to processing (including EEEs)
Dilute magnetic semiconductors
In-situ optical techniques
Thermal effects, more process-related studies in addition to microstructural studies
Bulk III-N growth and defects
Devices on Bulk III-N substrates
Quantum effects and devices of wide bandgaps (SiC, GaN…)
Sensors
Novel devices based on either new materials or new phenomena
WBG high power operations– stress/reliability/failure mechanisms
Extend this Workshop to include: theory (ists) specific to analysis
Multifunctional oxide interfaces, surfaces and defects
Interfacial effects, charge control and spatially-resolved, in situ diagnostics

Additional Comments/Suggestions:

- Success of the workshop was reduced by Martinez/DARPA threats to invitees, causing many cancellations.
- Riverside Inn is very well located. However, the hotel's operations are a bit unpolished, eg, one day my room was not made up, and another day I fixed a leaking toilet flapper myself. Also the sound insulation between our meeting room and the adjacent one was not good on Tuesday.
- Thanks!
- I wish the organizers could provide a copy of the transparencies of all the talks presented at this workshop.
- Some bottled water at breaks would be nice.
- "Outstanding Speaker" award should be "Outstanding Contributor" award.

- Riverside Inn outside telephone lines inadequate – front desk slow and ill-informed. Rafters was fine. Setting was excellent. More theory – even though difficult to find. Excellent conference!
- Great job, Shari!
- Great Workshop!
- Keep it up and keep it going. Only negative was the lack of sound proofing both in the rooms and in the seminar rooms.
- Overall – excellent.
- Great job -- excellent topic/speakers. Again, more time for one-on-one, one-on three conversations. Restrict attendance to only those willing to discuss ALL aspects of their work (this was done really well here).
- Make speakers put up a bond to insure attendance.

Rating on a Scale of 1 to 10, with 1 being poor, 10 being excellent:

Question	10	9	8	7	6	5	4	3	2	1	No Reply	Total
The Workshop met its stated goals and objectives.	5	9	10	1	0	0	0	0	0	0	1	8.7
Overall rating of the technical presentations.	4	10	10	2	0	0	0	0	0	0	0	8.6
Overall rating of the Riverside Inn.	0	1	7	10	3	2	1	0	1	0	1	6.8
Evaluation of the meeting planning services provided by Allwood & Associates, Inc.	20	4	1	1	0	0	0	0	0	0	0	9.6
Overall rating of the Workshop.	7	9	8	1	0	0	0	0	0	0	1	8.9

Tri-Services Workshop on Process Induced Defects in Wide Bandgap Semiconductors

MEETING PROGRAM, ABSTRACT BOOK & ATTENDEE ROSTER

August 17-21, 2003
Grants Pass, OR

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Program Schedule
Tri-Services Workshop on Process Induced Defects in Wide Bandgap Semiconductors

Please join us for the Welcoming Reception on Sunday evening, August 17th from 7:00 to 9:00 p.m. in the River Top Room. Spouses and guests are welcome!

Monday, August 18th, 2003	
Continental Breakfast: 7:30 - 8:00 a.m. – Rainbow/Chinook Rooms	
8:00 a.m. - 8:15 a.m. **Welcome & Orientation** – Co-chairs Drs. Brillson, Hu, Jones and Mitchel	
Session 1: Substrate-Induced Effects	**Chair: Bill Lampert**
8:15 a.m. – 8:45 a.m. (Scene-setter)	**Bob Davis:** The Influence of Domains, Lattice Parameters and Coefficients of Thermal Expansion in SiC(0001) Substrates on the Optical, Electrical, Mechanical and Microstructural Properties in Heteroepitaxial III-Nitride Films (Pg. 6)
8:45 a.m. - 9:05 a.m.	**Asif Khan:** Process Induced Defects in Non-Polar III-N Films (Pg. 8)
9:05 a.m. - 9:25 a.m.	**Alan Doolittle:** Process-induced changes in and elimination/creation of SiC surface & bulk defects for LiNbO3 and III-V Nitride Epi (Pg. 10)
9:25 a.m. – 9:45 a.m.	**Paul Fini:** Lateral Epitaxial Overgrowth of A-plane GaN by HVPE (Pg. 12)
9:45 a.m. – 10:05 a.m.	**Evelyn Hu**: GaN Wafer-bonded Interfaces: Electronic and Chemical Characterization as a Function of Bonding Temperature (Pg. 14)
Break: 10:05 a.m. – 10:25 a.m.	
Session 2: Etching, Implantation & Plasma Processing	**Chair: Bill Mitchel**
10:25 a.m. – 10:55 a.m. (Scene Setter)	**Umesh Mishra:** Problems and Benefits of a Reactive Ion Etched gate recess in AlGaN/GaN HEMTs (Pg. 16)
10:55 a.m. – 11:15 a.m.	**Deepak Selvanathan:** Wet and Dry Etching of III-Nitrides and Defect Observation (Pg. 18)
11:15 a.m. – 11:35 a.m.	**Dan Johnstone:** RIE Damage Studied by Photovoltage and Photoluminescence (Pg. 20)
11:35 a.m. – 11:55 p.m.	**Katherine Bogart:** Plasma Processing Induced Contact Defects in High %Al n-type AlGaN for UVLEDs (Pg. 22)
11:55 a.m. – 12:15 p.m.	**Discussion Time**
Lunch: 12:15 p.m. – 1:15 p.m. – River Top Room	

Monday, August 18th, 2003, Continued	
Session 2: Etching, Implantation & Plasma Processing, Continued	
1:20 p.m. – 1:40 p.m.	**Zhaoqiang Fang:** Plasma-etching induced/enhanced deep centers in MOCVD-grown n-GaN (Pg. 24)
1:40 p.m. – 2:00 p.m.	**Mulpuri Rao:** Deep Levels in P-N Diodes and MESFETs made by Ion-implantation (Pg. 26)
2:00 p.m. – 2:20 p.m.	**Ken Jones:** Activation of Implanted Dopants in SiC (Pg. 28)
Session 3: Interface Defects & Ohmic Contacts	**Chair: Ken Jones**
2:20 p.m. – 2:50 p.m. (Scene-setter)	**Ed Yu:** From microscopic characterization to processes for defect mitigation in nitride semiconductors (Pg. 30)
2:50 p.m. – 3:10 p.m.	**Mike Spencer:** Characterization of GaN/AlGaN surfaces and their effect on device performance by Scanning Kelvin Probe (Pg. 32)
3:10 p.m. – 3:30 p.m.	**Suzanne Mohney:** Process Induced Defects in Contacts to Group III Nitride Semiconductors (Pg. 34)
3:30 p.m. – 4:00 p.m.	**Discussion time**
Group Outing – Depart hotel promptly at 4:30 from Rafters Restaurant to board a **Hellgate Jet Boat** for a ride through spectacular Hellgate Canyon. Stop at the OK Corral for a **Country Banquet Dinner**. Return to Riverside Inn at approx. 8:30 p.m.	

Tuesday, August 19th, 2003	
Continental Breakfast: 8:30 - 9:00 a.m. – Rainbow/Chinook Rooms	
Session 3: Interface Defects & Ohmic Contacts, Continued	
9:00 a.m. – 9:20 a.m.	**Bob Nemanich:** Processing-induced changes in GaN/insulator interface electronic states (Pg. 36)
9:20 a.m. – 9:40 a.m.	**Len Feldman:** Interface Trap Density Near the Conduction Band Edge of the 4H-SiC/Oxide Interface (Pg. 38)
9:40 a.m. - 10:00 a.m.	**Len Brillson:** Process-Induced Defects at SiC Surfaces and Metal Interfaces (Pg. 40)
10:00 a.m. - 10:20 a.m.	**Bill Mitchel:** Carbon Based Ohmic Contacts on N-type SiC (Pg. 42)
Break 10:20 a.m. – 10:35 a.m.	
Session 4: Process-Induced Traps: Current Collapse, Dispersion & Passivation Chair: Len Brillson	
10:35 a.m. – 11:05 a.m. (Scene-setter)	**Jim Speck:** Progress in Extended Defect Control in the RF-Plasma MBE Growth of GaN (Pg. 44)
11:05 a.m. - 11:25 a.m.	**James Cooper:** Effect of Process-induced Defects on SiC Power Device Performance (Pg. 46)
11:25 a.m. – 11:45 a.m.	**Karim Boutros:** Process-dependent Device Characteristics of GaN-Based HEMTs (Pg. 48)
11:45 a.m. – 12:05 a.m.	**Robert Fitch:** Passivation Effects on PCM/DC/RF Performance of AlGaN/GaN HEMT's (Pg. 50)
12:05 noon – 1:05 p.m. **Lunch – River Top Room**	
1:05 p.m. – 1:25 p.m.	**Gregg Jessen:** The Effects of Processing on Point Defects in AlGaN/GaN HEMTs with Correlation to Device Performance (Pg. 52)
1:25 p.m. - 1:45 p.m.	**Remis Gaska:** Trap Engineering for Suppression of Current Collapse in AlInGaN-based Field Effect Transistors (Pg. 54)
1:45 p.m. – 2:05 p.m.	**Steve Binari:** Bias-stress-induced current collapse in GaN HEMTs (Pg. 56)
2:05 p.m. – 2:25 p.m.	**Robert Fitch (presented on behalf of Tom Jenkins):** Aging and Degradation of AlGaN/GaN HFET's (Pg. 58)
2:25 p.m. – 2:45 p.m.	**Discussion time**
3:15 p.m. **Group outing – Rafting Trip. Depart lobby promptly at 3:15 p.m.** We'll be bussed to a nearby river where we'll enjoy a two-hour rafting trip (some whitewater involved). Estimated return to the hotel is 7:00 p.m. Dinner on own.	

Wednesday, August 20th, 2003	
Continental Breakfast: 9:00 – 9:30 a.m. – Rainbow/Chinook Rooms	
Session 5: Thermal and Electronic Stress	**Chair: Evelyn Hu**
9:30 a.m. – 10:00 a.m. (Scene-setter)	**Jim Choyke:** Nano-polytypes (Extended Stacking Faults) Induced in Ultrapure Epitaxial Films of 4H SiC when Grown on Heavily n-type Doped Substrates (Pg. 60)
10:00 a.m. – 10:20 a.m.	**Pirouz Pirouz:** Processing-induced Generation of Stacking Faults in 4H-SiC (Pg. 62)
10:20 a.m. – 10:40 a.m.	**Robert Okojie:** Thermoplastic Deformation and Stacking Faults in 4H- and 6H-SiC (Pg. 64)
Break: 10:40 a.m. – 10:55 a.m.	
10:55 a.m. – 11:15 a.m.	**Brian Skromme:** Processing-Induced Polytype Transformation in 4H-SiC (Pg. 66)
11:15 a.m. – 11:35 a.m.	**Marek Skowronski:** Doping-induced Stacking Faults in Hexagonal SiC Polytypes (Pg. 68)
11:35 a.m. – 11:55 p.m.	**Mary Ellen Zvanut**: Affect of oxidation and annealing on the defect levels in high purity semi-insulating 4H SiC (Pg. 70)
11:55 a.m. – 12:55 p.m. **Lunch – River Top Room**	
Group Outing: Winery Tour. Depart from lobby at 1:00 p.m. to visit three area wineries. Return to the Riverside Inn at approximately 6:00 p.m.	
Wrap-up Session: 6:15 – 7:15 p.m. – Rainbow/Chinook Rooms. The Wrap-up session provides an opportunity for participants to gather to summarize the findings/technical information shared throughout the week. It's also the last opportunity to obtain answers to questions that time may not have allowed during the session. All participants are requested to participate.	
Dinner: 7:30 – 9:00 p.m. Ma Ma Mia Pasta Dinner – River Top Room	

Thursday, August 21st, 2003	
8:30 a.m. – 10:00 a.m.	**Continental Breakfast/Collaboration – River Top Room** Join together for a final breakfast designed to ensure that you have made plans for future collaborations with colleagues.

The Influence of Domains, Lattice Parameters and Coefficients of Thermal Expansion in SiC(0001) Substrates on the Optical, Electrical, Mechanical and Microstructural Properties in Heteroepitaxial III-Nitride Films

Robert Davis, North Carolina State University

Silicon carbide wafers contain domains with varying size and degree of tilt. This microstructure is mimicked in GaN films deposited on AlN-containing buffer layers, and it masks most variations in the FWHM of the X-ray rocking curves of the former. The shape and FWHM in the GaN curves are determined both by domain tilting and dislocation broadening; the latter is dominant in areas of reduced tilt. Analyses of the on-and off-axis X-ray data acquired from these regions of lower tilt revealed the marked effect of the higher density of edge dislocations on broadening. This effect decreased with increasing GaN thickness due to dislocation annihilation. Photoluminescence and sheet resistance maps of the GaN films have been acquired. The correlation of this data with the domain microstructure of the underlying SiC(0001) wafers will be presented.

Atomic force microscopy (AFM) by several investigators has revealed hillocks on the surfaces of GaN films a result of the rotation of heterogeneous steps formed at pure screw or mixed dislocations which terminated on the (0001) surface. However, the effect of these defects on the flatness of the AlGaN/GaN interface, electron scattering and mobility in the 2-dimensional electron gas of HEMT devices is not commonly discussed.

The evolution of the strain in GaN layers grown by metalorganic vapor phase epitaxy on either AlN or $Al_xGa_{1-x}N$ (x=0.15) buffer layers previously deposited on 6H-SiC (0001) substrates has been investigated by varying the GaN layer thickness from one GaN bilayer to 4 microns. Increasing the thickness of the GaN grown on either substrate caused the state-of-stress of these biaxially stressed layers to gradually change from compression to tension with regard to both their average strain and their local strain along the [0001] growth direction. The components of both the compressive and tensile stresses are caused by the mismatch in lattice parameters between the GaN and the buffer layer and the mismatch in the coefficients of thermal expansion between GaN and SiC, respectively. The compressive stress is partially relieved within the first 20 nm in the GaN film grown on the AlN buffer layer. The relief of the remaining stress follows an exponential dependence on the thickness of the GaN layer with values for the characteristic decay length of 0.24 μm and 0.64 μm for the AlN and AlGaN buffer layer, respectively. The effect of the various strain states on device properties will be considered.

AlGaN films are important as a conductive buffer layer on SiC substrates and as a component of the device structure in, e.g., UV light emitting diodes and HEMT devices. However, the biaxial stresses imposed on these layers for the reasons noted above can result in micro-phase separation of areas of high and low concentrations of AlN and GaN. The effects of this phenomenon, when it occurs, on device properties are believed to be unknown; however, possibilities will be raised for audience discussion.

NOTES

Process Induced Defects in Non-Polar III-N Films

M. Asif Khan
University of South Carolina

Due to the absence of polarization fields that result in band-bending which reduces the emission efficiency, there is a renewed interest in non-polar III-N films and heterostructures. Several groups have now reported the growth on non-polar a-plane GaN-AlGaN-InGaN films, heterostructures and quantum wells over r-plane sapphire substrates. The non-polar GaN films over r-plane sapphire in general have a large number of threading dislocations and stacking faults. These defects have a significant impact on the optical and electrical properties.

Recently we have developed a new selective area lateral epitaxy process (SALE) to significantly reduce these defects in the non-polar GaN films over r-plane sapphire substrates. We have also used these low defect films as templates for a subsequent deposition of InGaN-AlInGaN MQW LED structures. The materials and devices were studied to determine the type of defects and dislocations and their impact on the resulting device performance.

In this paper we will present the results of our studies with specific emphasis on the defects that are generated from the growth and the fabrication processes employed for the device epitaxial layers. Data will also be presented to elucidate the approaches that were developed to control the defect formation and propagation through the structures.

NOTES

Process-induced changes in and elimination/creation of SiC surface & bulk defects for $LiNbO_3$ and III-V Nitride Epi

W. Alan Doolittle

The role of surface, point, and extended defects in SiC influences the success of subsequent epitaxial layers grown on them including SiC, III-Nitride, and recently lithium niobate. Understanding and elimination of the process induced damage effecting subsequent epitaxy is extremely important. In this presentation, several experimental observations will be presented related to the observation/evolution of surface, point and extended defects in SiC. These include the observation and difficulties in accurately characterizing very high concentration point defects in SiC via DLTS, the creation of and modification of electrical activity of defects when using electron beam probing techniques in an SEM. Additionally, the ability to improve on the surface roughness of an as-delivered SiC wafer using novel vacuum based approaches.

NOTES

Lateral Epitaxial Overgrowth of A-plane GaN by HVPE

P. Fini, B.A. Haskell, S. Matsuda*, F. Wu, M.D. Craven, S.P. DenBaars, J.S. Speck, and S. Nakamura

Materials Dept., Univ. of California Santa Barbara; Santa Barbara, CA 93106

** now at the Japanese Patent Office, Tokyo, JAPAN*

We report on the reduction in extended defect densities in a-plane $\{11\bar{2}0\}$ GaN films achieved via lateral epitaxial overgrowth by hydride vapor phase epitaxy. A variety of stripe patterns and directions were used to produce 8-125 μm-thick, fully coalesced nonpolar GaN films. The nanometer-scale surface pit densities in the overgrown regions ('wings') were less than $3x10^6$ cm^{-2} compared to $>10^{10}$ cm^{-2} in the direct-growth ('window') GaN. Cathodoluminescence revealed a fourfold increase in luminous intensity in the wing material compared to the window material. X-ray rocking curves indicated the films were free of wing tilt within the sensitivity of the measurements. Whereas non-LEO a-plane GaN often exhibits basal plane stacking fault and threading dislocation densities of $\sim10^5$ cm^{-1} and $>10^9$ cm^{-2}, respectively, the overgrown LEO material was generally free of extended defects. The basal plane stacking fault and threading dislocation densities in the wing regions were below the transmission electron microscope detection limits of $3x10^3$ cm^{-1} and $\sim5x10^6$ cm^{-2}, respectively.

NOTES

Problems and Benefits of a Reactive Ion Etched gate recess in AlGaN/GaN HEMTs

Umesh Mishra

University of California at Santa Barbara

Dry Etching of the (Al,GaN)N material system will emerge as important for advancement in device performance as proven in an analogous fashion in Si and the conventional III-V materials. We have studied the Reactive Ion Etching of these materials extensively as a function of power, pressure and chamber environment. In the talk I will present details of these findings. Stated succintly, GaN and AlGaN etch rather nicely in Chlorine. Any oxygen in the chamber introduced in any manner kills the reproducibility of the process. Removing oxides on the surface and oxide containing materials anywhere in the chamber is therefore crucial, Low power etching is the key to maintaining a low leakage from schottky barriers deposited on etched surfaces. Though the end result is simple and very promising it is the result of sucking the last drops of blood out of two extremely talented researchers.

NOTES

Wet and Dry Etching of III-Nitrides and Defect Observation

D. Selvanathan, F. A. Khan, V. Kumar, H. K. Cho and I. Adesida
Micro and Nanotechnology Laboratory, University of Illinois at Urbana-Champaign, Urbana, Illinois – 61801.

The inertness of GaN-based semiconductors dictates that techniques involving incident energies are required for etching them. To this end we have developed both wet and dry methods for etching GaN materials. A photoelectrochemical (PEC) etching technique for GaN using an ultraviolet (UV) light source for illumination and an electrochemical cell with potassium hydroxide as the electrolyte is used for wet etching of n-GaN. Several types of surface morphologies, varying from smooth surfaces, whisker formation to hexagonal pit formation, have been observed on etched materials. These morphologies are dependent on the pH of the electrolyte and the intensity of the UV illumination. Whisker formation on the surface of GaN is related to the dislocations in the material and thus this technique can be used as an effective tool to measure the dislocation density.

Inductively-coupled-plasma reactive ion etching (ICP-RIE) has been developed for producing highly anisotropic profiles in GaN. The inherent problem with ICP-RIE much like other dry etching methods involving ion bombardment is the creation of defects. We have studied systematically the effects of Cl_2/Ar plasma etching of GaN in an ICP-RIE system using Schottky barrier height measurements. Presently, we are working on studying the nature of defects formed during ICP etching of GaN using deep level transient spectroscopy (DLTS) measurements and preliminary results will be reported at the workshop. The efficacy of anneal treatments to remove plasma-induced damage will also be discussed. The long-term aim of this study is to better understand the effects of defects on the performance characteristics of GaN-based devices.

NOTES

GaN Wafer-bonded Interfaces: Electronic and Chemical Characterization as a Function of Bonding Temperature

E.L. Hu, S. Estrada, U. Mishra; UCSB

Wafer fusion, or direct bonding of lattice-mismatched materials, has provided a means to improve device performance through separate optimization of the component materials. Fusion of GaAs and InP materials has produced efficient vertical cavity lasers, and fusion of InGaAs and Si has formed high quality avalanche photodiodes. Wafer fusion incorporating GaN may allow creation of new optical or electronic devices, or may be used to bring about thermal or strain management. We have explored the use of wafer fusion to form (Al)GaAs-GaN heterostructure bipolar transistors, where the n-GaN comprises the collector and the n-AlGaAs, and p-GaAs form the emitter and base, respectively. Systematic variations of the temperature and time of fusion show the formation of mechanically stable fused junctions at temperatures as low as 550°C. Transmission electron microscopy (TEM) reveals that a large fraction of the interface area is well-bonded, with the presence of a thin (1-2 nm) amorphous layer of a native oxide at the bonded interface. Chemical analysis of the junction reveals accumulations of dopants at fused interface, even for the lowest fusion temperatures. Substantial oxygen and carbon are also localized at the interface. Increased temperature results in a decrease in the peak height at the junction, but with substantial diffusion into the GaAs layer. I-V characteristics of the HBT show a general degradation with increasing fusion temperature.

NOTES

RIE Damage Studied by Photovoltage and Photoluminescence

S. Sabuktagin, M. A. Reshchikov, S. Dogan, S.-J. Cho, D. Johnstone, and H. Morkoç
Virginia Commonwealth University, Richmond, VA 23284

GaN-based optical and electronic devices have been developed rapidly in recent years, however little attention has been given to the properties of GaN surface, as-grown and treated for device fabrication. The surface of undoped GaN is known to exhibit an upward band bending of the order of 1 eV [1], whereas the exact value depends on the surface treatment. We studied how reactive ion etching (RIE) affects the surface of undoped GaN using photoluminescence (PL), atomic force microscopy (AFM), and electric-force microscopy (EFM), in the dark and under UV illumination (Photovoltage) methods. The effects of different surface treatment, such as boiling in aqua-regia and brief etching in molten KOH on as-grown and RIE-treated surfaces were also investigated. From the surface potential, we have estimated an upward band bending of about 0.7 eV in as-grown GaN. The band bending in GaN treated by RIE was about 1.0 eV, which we explain by creation of additional surface states. Illumination with UV light decreased the band bending by about 0.4 eV. However, the dynamics of this decrease, as well as the dynamics of the barrier height increase after switching off the UV light source was very different in as-grown and RIE-treated samples. The surface potential rise and decay were on the order of seconds for the as-grown case, and very slow (minutes to hours) for the RIE etched case. This observation also supports the assumption about high density of the surface states created by RIE. Brief etching in molten KOH did not affect the surface morphology appreciable from analysis of the AFM images, however it apparently removed the RIE damage since the dynamics of the surface potential under pulse UV illumination became nearly the same as in as-grown samples. Low-temperature PL spectrum in as-grown GaN contained intense exciton-related peaks and yellow luminescence more than three orders of magnitude weaker than the exciton peaks. After RIE, the shape of the spectrum was unchanged, whereas the intensity dropped 3 to 4 times. This effect can be attributed to creation of nonradiative defects near the surface of the RIE-treated GaN.

[1] V. M. Bermudez, J. Appl. Phys. **80**, 1190 (1996).

NOTES

Plasma Processing-Induced Contact Deficiencies in High %Al *n*-type AlGaN

K.H.A. Bogart, A.J. Fischer, M.H. Crawford, D.D. Koleske, A.A. Allerman, R.J. Shul, and D.E. Peebles

Katherine H. A. Bogart
Principal Member of Technical Staff
Chemical Processing Science Department
Sandia National Laboratories
Albuquerque, NM 87185
khbogar@sandia.gov

AlGaN alloys are suitable for a variety of light emitting devices including LEDs and laser diodes as well as electronic devices such as high electron mobility transistors. Deep UV (<300 nm) LEDs have important applications as UV light sources for chemical-biological sensors, non-line-of-sight optical communications, and UV curing. Optical performance near 300 nm requires a Group III Al stoichiometry of 0.25 to 0.5, or more. The difficulty of forming high-quality ohmic contacts to n-type AlGaN materials increases with increasing percent Al due to the difficulty in effectively doping high percent aluminum AlGaN, dislocation defects, and surface oxidation. For example, during LED device processing, plasma etching of the p-type material and the active material is done in order to access the underlying n-type material for contact formation. We have observed that Ti/Al/Ni/Au contacts on as-deposited n-type $Al_{0.47}Ga_{0.53}N$ are ohmic, but are Schottky on the same material that has been etched in a high-density plasma. The contact quality improves with annealing, but not to the point of displaying ohmic behavior. For n-GaN, plasma etching has been shown to improve the contact performance due to the formation of nitrogen vacancies, thus increasing n-type carrier concentration.[1,2,3,4,5] For some high percent aluminum (Al >47%) n-AlGaN material, we have observed that the plasma etching process renders n-type contacts non-Ohmic. This process-induced detrimental effect on contact performance is currently under investigation through compositional and morphological analysis of the as-deposited and plasma etched surfaces, by pre-metallization surface treatments[3] and post-metallization anneals, and by electrical and optical characterization of the material films and resulting devices, as a function of percent Al ranging from 0 to 60%. We determined the effect of percent Al in AlGaN alloys on the surface roughness, etching rates, and resist selectivity, as a function of plasma etch method (ICP vs. RIE) and etching parameters such as substrate bias voltage. We also varied the pre-metallization surface treatments using dry plasma etching and wet chemical (BOE and HCl) etching. We evaporated metal contacts of either Ti/Al/Ni/Au or Ti/Al/Mo/Au and determined specific contact resistance as a function of percent Al (0 to 60%). Annealing studies were also performed on materials after the contact deposition. Surface analysis by XPS, performed before and after plasma etching showed striking stoichiometric differences between the as-grown alloy and the etched surface. The composition of the metal-AlGaN interface was also investigated by XPS. The results from all of these studies will be presented.

1. S. J. Pearton, J. C. Zolper, R. J. Shul, F. Ren, J. Appl. Phys. **86** 1 (1999)
2. R. J. Shul, L. Zhang, A. G. Baca, C. G. Willison, J. Han, S. J. Pearton, F. Ren, J. Vac. Sci. Technol. A **18** 1139 (2000)
3. A. T. Ping, Q. Chen, J. W. Yang, M. Asif Khan, I. Adesida, J. Electron. Mater., **27** 261 (1998)
4. A. T. Ping, A. C. Schmitz, I. Adesida, J. Electron. Mater. **26** 266 (1997)
5. V. Kumar, L. Zhou, D. Selvanathan, I. Adesida, J. Appl. Phys. **92** 1712 (2002)

NOTES

Plasma-etching induced/enhanced deep centers in MOCVD-grown n-GaN

Z-Q. Fang and D.C. Look
Semiconductor Research Center, Wright State University, Dayton, Ohio 45435

GaN is an excellent material for fabricating novel devices, which include GaN-based LEDs and AlGaN/GaN heterostructure field-effect transistors. Due to GaN's inert chemical nature and high bond energies, it is resistant to most wet chemical etchants, making device patterning mostly dependent on plasma etching. Plasma-etching induced damage has been studied mainly by analyzing current-voltage (I-V) characteristics of Schottky barrier diodes (SBDs) made on the damaged GaN surface, in conjunction with various surface stoichiometry analyses, such as X-ray photoelectron spectroscopy and Auger electron spectroscopy. It is believed that the degraded I-V characteristics are associated with etching-induced defects, which however have not yet been clearly elucidated. In this presentation, we use deep level transient spectroscopy (DLTS) to demonstrate that a well-known trap is strongly enhanced in n-GaN by plasma etching. An important conclusion is that this trap must be defect related.

Using deep level transient spectroscopy (DLTS), deep centers have been characterized in SBDs made on unintentionally doped n-GaN samples grown by the MOCVD technique and subjected to inductively coupled plasma (ICP) reactive ion etching. At least six commonly observed DLTS traps exist in the control sample: A_1 (~0.90 eV), A_x (~0.72 eV), B (0.61 eV), C_1 (0.44 eV), D (0.25 eV), and E_1 (0.17 eV), with B a dominant one. However, in ICP etched samples, as the etching bias-voltage increases from –50 to –150 V, trap D increases strongly and becomes dominant while traps A_1, C (0.34 eV), and E_1 increase at a slower rate. These traps were found to be located near the surface region. Trap B, on the other hand, is nearly unchanged. Previous electron-irradiation studies are consistent with the E_1 traps being N-vacancy related. It is likely that the D traps are also, except that they are in the regions of dislocations, behaving as "line-defects".

Future work will examine annealing effects, and also variations that might arise due to growth technique, and dislocation type and density.

NOTES

Deep Levels in P-N Junction Diodes and MESFETs Made by Ion-implantation

S. Mitra and Mulpuri V. Rao, Dept. of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030-4444; K. A. Jones, Army Research Laboratory, Adelphi, MD 20783-1197; N. Papanicolaou, Naval Research Laboratory, Washington, D.C. 20375.

Ion-implantation is an attractive method for selective area doping of planar SiC devices. Using SiO_2 layers as implant blocking layers, for elevated temperature (700 °C) implants, we have made p^+-n (n^+-p) junction diodes by a deep range donor (acceptor) followed by a shallow range acceptor (donor) ion-implantation schedules in n-type (p-type) 4H-SiC epitaxial layers. Double ion-implantations of this nature are very useful in making complimentary FETs, thyristors etc. We also made n-channel MESFETs in semi-insulating bulk 4H-SiC substrates by a room-temperature selective area nitrogen ion-implantation schedule. Source/drain and channel regions are all created by ion-implantation in the bulk SI substrate. Deep level trap measurements were performed on these devices by using capacitance deep level transient spectroscopy (DLTS). The trap results are correlated with device current-voltage characteristics.

The p+-n junction diodes, made by a deep range nitrogen or a phosphorus implantation schedule followed by a shallow range aluminum implantation schedule at 700 °C, and annealed for 10 min. at 1600-1650 °C, have a high trap density than the n^+-p junction diodes made by a deep range boron or aluminum implantation followed by a shallow range nitrogen ion-implantation. The dark reverse bias leakage currents of the junction diodes are greater in the diodes with a higher trap concentration. In these diodes, a dominant nitrogen-defect complex center is observed at E_v + 0.51 eV and a boron related D-center at E_v + 0.63 eV. The nitrogen dopant- native defect center complex trap at E_v + 0.51 eV and a V related trap at E_v + 0.6 eV are seen in capacitance DLTS measurements on Al gate – nitrogen implanted channel Schottky junction. Several high-density traps, related to the Al ion and P ion implantations, are also observed. In p^+-n junction diodes, the trap density is in the order of 10^{18} cm^{-3}, resulting in a mA/cm^2 range reverse leakage current, where as, several orders lower ($\mu A/cm^2$ range) reverse leakage current was measured in the n^+-p junction diodes. A high degree of residual implant damage left by the heavier Al ion-implantation of the p+ region compared to the lighter N ion-implantation of the n+ regions is considered responsible for this I-V behavior.

We also observed a monotonically increasing E_v + 0.51 eV trap density from the channel surface towards the channel/substrate interface and also from inside the bulk substrate towards the channel/substrate interface. These traps that are present at the implanted region/substrate interface strongly influence the channel carrier mobility and thus the device performance. Transconductance frequency dispersion measurements were also performed on the fully implanted MESFETs to observe bulk as well as the surface traps in the channel region. Surface traps of the ungated channel region between the source and gate and gate and drain were observed at 0.18 eV, 0.3 eV and 0.4 eV above the valence band edge.

NOTES

Activation of Implanted Dopants in SiC

K.A. Jones, M.H. Ervin, T.S. Zheleva, P.B. Shah, M.A. Derenge, Army Research Lab;
J.A. Freitas, Naval Research Lab; and R.D. Vispute, University of Maryland

Implantation activation is a particularly important issue for SiC because it cannot be doped effectively by thermal diffusion as the rate of diffusion of most dopants is too slow even at temperatures as high as 1800°C. The activation process, however, is not as effective as it is in other semiconductors as the carrier mobilities are always much less than they are in an epitaxial film doped to the same level, and it appears to be very difficult, if not, impossible, to fully activate the implants. The activation process can be facilitated at lower annealing temperatures by co-implanting C, but still the activation is far from complete. It is important to understand what is happening on a fundamental level as, not only could it provide insight into how to increase the degree of activation, it could also provide insight into why e.g. implanted p-n junctions have larger leakage currents, and possibly why there are of the lower channel mobility in ion implanted 4H-SiC MOSFET's.

Our AlN anneal cap provides us a unique opportunity to study these effects as it prevents the preferential evaporation of Si at the high temperatures required to activate the implants, which roughens the surface and generates additional defects. It is particularly important for our studies that the near surface region not be disturbed because one of our experimental techniques for probing the annealed structures is RBS/ channeling spectroscopy, which probes only the material within the top few tens of nm of the surface. Using a BN/AlN cap, we have demonstrated that the surface of the SiC remains pristine even after annealing at temperatures as high as 1700°C for times as long as 30 minutes.

In this paper we discuss the effects of implanting Al, Al and C, or Al and Si and annealing samples at 1400, 1500, 1600, 1650 or 1700°C for 30 min after they have been capped with AlN and BN films. The material is examined electrically measuring the sheet resistance, R_{sh}, at different temperatures; optically by recording their low temperature cathodoluminescence (CL) spectra; and structurally by measuring the relative amount of channeling as well as examining the microstructure using transmission electron microscopy (TEM). We show that C facilitates and Si impedes the reaction for the incorporation of Al into the SiC lattice at the lower, but not the higher, annealing temperatures. Our CL data suggest that the apparent degree of electrical activation is less than expected because some of the acceptors are trapped out by an implantation induced defect – possibly the D_I defect. We also show that the higher energy CL peak in the D_I doublet increases with the annealing temperature and with the amount of initial implant damage, and speculate that this is due to increasing the density of states associated with this peak. The initial decrease in the amount of channeling and subsequent increase as the annealing temperature increases seen in our RBS results suggests that some structural defects nucleate and grow, and our TEM results show that they are stacking faults. We believe that these stacking faults, which can be viewed as 3C and/or 6H domains imbedded in the 4H-SiC lattice, account for the lower mobility in ion implanted structures, and speculate that they, acting as nanoparticles, they might be the source of the CL peaks associated with the D_I defect.

NOTES

From microscopic characterization to processes for defect mitigation in nitride semiconductors

E. J. Miller, D. M. Schaadt, and E. T. Yu

Department of Electrical and Computer Engineering, University of California at San Diego
La Jolla, CA 92093-0407

The heteroepitaxial nature of most nitride semiconductor growth – typically on sapphire or SiC substrates – leads to high concentrations of dislocations and other defects in nitride semiconductor thin films. Subsequent processing for device fabrication can lead to the generation of additional defects or, in some cases, to elimination or mitigation of deleterious defect-related electronic behavior. We will discuss a variety of scanning-probe-based techniques for characterization at the micron to nanometer scale of electronic properties associated with growth- or process-induced defects in nitride semiconductors, and the development, based on the understanding resulting from application of these characterization methods, of a processing technique for mitigation of leakage currents arising from dislocations in GaN grown by molecular-beam epitaxy (MBE).

Specifically, we will describe the use of atomic force microscopy, scanning capacitance microscopy, scanning Kelvin probe force microscopy, conductive atomic force microscopy, and related techniques to assess local electronic properties arising from the presence of defects; these approaches enable direct imaging of electronic structure with spatial resolution of ~10-100nm laterally and at the nanometer scale in depth. Imaging of localized carrier depletion and surface potential modulation associated with individual, negatively charged threading dislocations, and of highly localized vertical conduction paths associated with dislocations in MBE-grown GaN, will be presented as illustrative examples. We will then discuss, in greater detail, the imaging and characterization of dislocation-related conduction paths in MBE-grown GaN, their relation to high leakage currents typically observed in these materials, and the resulting discovery of a microscopic mechanism for suppression of these leakage currents. The subsequent development of a simple electrochemical process for implementation of this suppression mechanism on a macroscopic scale will then be presented. Reductions in reverse-bias leakage current in Schottky contacts to n-GaN by a factor of 10^3 or more are achieved, accompanied by improvements in diode ideality factor from ~1.7-1.8 to ~1.1. Detailed studies of defect-related leakage current mechanisms, their mitigation, and compatibility of this process with other typical device fabrication processes will also be addressed.

NOTES

Characterization of GaN/AlGaN surfaces and their effect on device performance by Scanning Kelvin Probe

M. G. Spencer
Dept. of Electrical and Computer Engineering Cornell University,
Ithaca New York 14853

III-nitride based heterostructure field effect transistors (HFETs) have been the focus of intense research for the last few years. This is in part due to the high microwave output power that can be obtained from these devices. The formation of AlGaN/GaN heterostructure results in a very high two-dimensional electron gas (2DEG) concentration at the interface even in absence of any intentional doping due to the piezoelectric properties of the nitrides. Presence of such a high 2DEG in addition to high breakdown electric field of III-nitrides results in output power densities of 11-12 W/mm, roughly an order of magnitude higher than that achievable from GaAs based devices. However, for GaN based devices one of the technological challenges is the device performance degradation at high frequencies under high bias stress. This results in much lower output power density than expected from the static I-V characteristics. Various theories have been proposed to explain such a reduction in output power (commonly called current collapse or current slump) density based on buffer layer electron trapping, vertical gate field, and surface state electron trapping. While no clear consensus exists on the actual reason for current slump, it has been widely observed that the output power performance improves quite dramatically after passivating the exposed surface of the device with SiN_x. This suggests a significant role played by the surface in device performance. In this work nitride HFET devices have been stressed and the change in surface potential has been measured using scanning Kelvin probe microscopy (SKPM). The changes in surface barrier height can be measured by SKPM as a function of both distance and time. For undoped samples, assuming no significant charge in the AlGaN layer, the surface barrier height is directly related to the charge dipole across the AlGaN layer. Therefore, an increase in surface barrier results in a decrease in 2DEG concentration. Simultaneous surface potential and drain current measurements have been conducted to verify the effect of surface potential change on 2DEG concentration. In addition to the device samples studies of the surface barrier potential have been on unprocessed material. Both passivated and unpassivated samples have been studied in this work and compared. The effect of UV illumination has also been studied. In addition preliminary studies of reliability of these devices have been conducted using these techniques

NOTES

Process Induced Defects in Contacts to Group III Nitride Semiconductors

Suzanne Mohney
The Pennsylvania State University

Physical vapor deposition of contact metallizations can introduce electrically active defects in the group III nitride semiconductors, as we have previously reported for Pt Schottky barrier contacts to n-type GaN. These defects lead to enhanced reverse currents and reduced effective barrier heights of the diodes. Depending on whether the contacts are sputtered or deposited by electron beam evaporation, a variety of levels within 0.9 eV of the conduction band edge are created, as determined by deep level transient spectroscopy. It is possible to minimize the creation of these defects, however, through the selection of physical vapor deposition parameters. Furthermore, electrochemical deposition does not lead to the creation of detectable defects within the semiconductor.

More recently we have examined the effect of high temperature processing on contact metallizations to the group III nitride alloy semiconductors. The reaction of late transition metals such as Ni and Pd with AlGaN at high temperatures leads to a compositional shift in the semiconductor immediately beneath the contact metal, as determined by x-ray photoelectron spectroscopy and scanning transmission electron microscopy. Consistent with the thermodynamic driving forces in these systems, Ga is preferentially incorporated into the contact, and the Al/Ga ratio in the semiconductor immediately beneath the contact is enhanced. Interestingly, the same annealing conditions at which this compositional shift is initiated are those that we have found to result in enhanced current transport in contacts to Mg-doped AlGaN. Nevertheless, we would not expect the formation of a graded interfacial layer enriched in AlN to enhance current transport in contacts to p-type AlGaN, based on the anticipated band line-up or polarization effects. We therefore suspect that electrically active defects are created within the AlGaN during the outdiffusion of Ga from AlGaN, and we have begun to examine this issue through collaborations with other researchers.

NOTES

Processing-induced changes in GaN/insulator interface electronic states

R. J. Nemanich, T.E. Cook, Jr., C.C. Fulton, W.J. Mecouch, R.F. Davis, G. Lucovsky
Department of Physics, and Department of Materials Science and Engineering
North Carolina State University
Raleigh, NC, 27695-8202, USA

The characteristics of clean n- and p-type GaN (0001) surfaces and the interface between this surface and SiO_2, Si_3N_4, and HfO_2 have been investigated. Layers of SiO_2, Si_3N_4, or HfO_2 were carefully deposited to limit the reaction between the plasma and clean GaN surfaces. After stepwise deposition, the electronic states were measured with x-ray photoelectron spectroscopy (XPS) and ultraviolet photoemission spectroscopy (UPS). A valence band offset (VBO) of 2.0 eV with a conduction band offset (CBO) of 3.6 eV was determined for the GaN/SiO_2 interface. The large band offsets suggest SiO_2 is an excellent candidate for passivation of GaN. For the GaN/Si_3N_4 interface, type II band alignment was observed with a VBO of 0.5 eV with a CBO of 2.4 eV, which differs substantially from prior reports. We suggest that the differences are related to the level of oxygen incorporated at the interface. A VBO of 0.4 eV with a CBO of 2.0 eV was determined for the GaN/HfO_2 interface. An instability was observed in the HfO_2 film, with energy bands shifting ~0.5 eV during a 650°C densification anneal. The deduced band alignments were compared to the predictions of the electron affinity model and deviations were attributed to a change of the interface dipole. The largest deviation was observed for the oxide layers. It was noted that the existence of Ga-O bonding at the heterojunction can significantly affect the interface dipole, and consequently the band alignment in relation to the GaN.

NOTES

Interface Trap Density Near the Conduction Band Edge of the 4H-SiC/Oxide Interface

L. C. Feldman[1,2], S. Dhar[1], Y. W. Song[2], S.T Pantelides[2]

[1]Interdisciplinary Materials Science, [2]Dept. of Physics and Astronomy,

Vanderbilt University, Nashville, Tennessee 37235

T. Isaacs-Smith, C. C. Tin and J. R. Williams

Physics Department, Auburn University, Auburn, Alabama 36849

G. Chung

Dow Corning Corp., Tampa, FL 33619

E. Garfunkel[3] and T. Gustafsson[4]

[3]Dept. of Chemistry, [4]Dept. of Physics, Rutgers University, New Jersey 08854

Wide band gap, isotropic bulk electron mobility and native oxide (SiO_2) make the 4H polytype of silicon carbide a promising material for power switching applications. However historically, inversion-mode 4H-SiC MOSFETs have been characterized by lower-than-expected electron channel mobility as the result of a high interface trap density near the SiC conduction band edge. Over the past few years, our group and others have reported substantial progress in the passivation of the 4H-SiC/SiO_2 interface state density using post-oxidation anneals in various gases such as ammonia, nitric oxide and nitrous oxide, and more recently hydrogen. Anneals in nitric oxide (NO) reduce the interface trap density at 0.1-0.2eV below the band edge from well above $10^{13}cm^{-2}eV^{-1}$ to $\sim 10^{12}cm^{-2}eV^{-1}$, with corresponding increases in channel mobility from single digits to 40-50cm^2/V-s. This talk will focus on the correlation of interface structure and chemistry with the modified interface, the crystal face dependence of the oxidation process and the needs and possibilities for further improvements.

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NOTES

Process-Induced Defects at SiC Surfaces and Metal Interfaces

Leonard J. Brillson
The Ohio State University, 205 Dreese Lab, 2015 Neil Ave., Columbus, OH 43210

R. S. Okojie
NASA Glenn Research Center, 21000 Brookpark Road, M/S 77-1, Cleveland, OH 44135

M. Zhang and P. Pirouz
Case Western Reserve University, Cleveland, OH 44106

Electron-excited luminescence studies of SiC surfaces and interfaces provide evidence for localized states that can influence charge transfer at metal-SiC junctions. These states can have major effects on Schottky barriers, ohmic contacts, free carrier confinement and recombination - with adverse consequences for the power and speed of microelectronics. Yet little is know about the electronic properties of these states and their dependence on chemical or thermal processing. We have employed nanometer-scale, depth-resolved, low energy cathodoluminescence spectroscopy to show the variable nature of these states at the intimate metal-semiconductor contact with different chemical treatments and hence their strong sensitivity to local chemical bonding. Bare surface annealing of highly doped (10^{19} cm^{-3} N) 4H-SiC at high temperatures (1150°C) produces deep level emissions at 2.5 and 1.9 eV corresponding to 3C-like stacking fault regions[1] and dislocations decorating their boundaries, respectively. Annealing in argon at these temperatures and dopings produces similar features, confirming the intrinsic nature of these electronic states. Pt/Ti overlayers on S-face 4H- and 6H-SiC in general exhibit a continuum of states across the band gap, deep level emission at 2 eV (1.9 eV) for 4H (6H) –SiC, reduced symmetry polytype formation - all within 10 -20 nm of the interface. For the 2.93 eV 6H-SiC energy gap, the band gap complement of this 1.9 eV emission energy equals 1.03 eV, close to the Schottky barrier of 0.93 – 0.97 eV for Ti on the Si face of 6H-SiC after annealing, as well as Si-face Schottky barrier for Pt of 1.06 eV for as-deposited metal.[2]

Annealed metal – 4H-SiC junctions also generate discrete states in this interface region. Thus Au on 4H-SiC annealed at 800°C produces deep level emissions at ~ 2 eV and 2.7-2.9 eV within nanometers of the junction. Defect emission at the Ni-4H-SiC junction changes from 1.8 eV at 600 °C to 2.8 eV at 900°C. The similar energies of these emissions with different surface treatments and metallizations and the correspondence with their 4H-SiC Schottky barriers[3] indicates that native defects influence the barrier formation, despite the electronic and chemical differences between these metals. Nevertheless, they depend on the extent of interfacial reaction. Thus, the interplay between structural and chemical effects in the near-interface region has significant implications for the processing of SiC devices and highlights the control of defects required at the nanoscale interface.

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NOTES

Carbon Based Ohmic Contacts on n-type SiC

W. C. Mitchel[1] and Weijie Lu[2]

[1]Air Force Research Laboratory/Materials and Manufacturing Directorate
AFRL/MLPS
Wright-Patterson AFB, OH 45433-7707

[2]Fisk University
Department of Physics
Nashville, TN 37208

The mechanisms by which ohmic contacts are formed on SiC are still not fully understood. It is well known that after the deposition of contact metals and annealing of the structure silicides and free carbon are often formed. However, chemical analysis shows that the silicides form at much lower temperatures than are required to activate ohmic conduction. We report here an investigation of the electrical properties of bare carbon films deposited on n-type SiC substrates and metal/carbon/SiC structures. Raman scattering was used to determine the structure of the free carbon. Both I-V measurements of dot structures and transmission line measurements were used to measure the electrical properties. Annealing was performed in Ar at temperatures up to 1350°C. As deposited bare carbon films were rectifying but became ohmic after 1050°C to 1350°C. Specific contact resistance varied from 10^{-3} to 10^{-4} Ωcm^2 depending on the doping level of the substrate. Raman scattering measurements showed that as deposited films were amorphous. Small scale graphite structures were found after high temperature anneals that convert the contacts from rectifying ohmic. The effect of free carbon on metal based ohmic contacts was investigated by depositing various metals on top of carbon films deposited directly on to n-type SiC substrates. Ni/C/SiC contacts went ohmic after anneals at temperatures as low as 700°C for $1x10^{19}$ cm^{-3} doped material. The lowest specific contact resistance measured on Ni/C/SiC structures was $7x10^{-7}$ Ωcm^2 for a $3x10^{19}$ cm^{-3} doped substrate after 800°C anneals. Raman measurements indicated the presence of graphite in these structures at much lower annealing temperature than for bare carbon films and again the formation of small scale graphite platelets corresponded to the ohmic contact activation energy. Other metals that produced ohmic contacts with carbon on n-type SiC were Co and Cr. Al, Au, Mo, Ti and W films on carbon remained rectifying after two hours at 800°C. All the metals that formed ohmic contacts with carbon are known to be catalysts for the formation of graphite from other forms of carbon. We speculate that surface states on small graphite platelets are responsible for the ohmic contacts on our structures and that carbon might play a more important role in the formation of ohmic contacts in general than was previously believed.

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NOTES

Progress in Process Control in the Plasma-Assisted MBE Growth of GaN

James S. Speck
Materials Department
University of California
Santa Barbara, CA 93106
Tel: (805) 893-8005, Fax: (805) 893-8983, e-mail: speck@mrl.ucsb.edu

In this talk, we review the process issues associated with the direct III-nitride growth of GaN on SiC by plasma-assisted molecular beam epitaxy (RF-MBE). We summarize our experience on SiC substrate surface preparation, backside metallization, temperature growth process strategies (temperature control and uniformity) and layer optimization. We highlight recent work on *in situ* diagnostics for growth process control, strain gradients, and carbon doping.

NOTES

Effect of Process-induced Defects on SiC Power Device Performance

James A. Cooper, Jr.
School of Electrical and Computer Engineering
Purdue University, West Lafayette, IN

Silicon carbide (SiC) offers significant advantages over silicon for power switching devices, due primarily to its 10x higher critical field for avalanche breakdown. Over the past ten years, our group has grappled with the technological challenges in realizing the full potential of SiC power devices. This talk will deal specifically with the effect of process-induced defects on the performance of SiC power MOSFETs and bipolar transistors (BJTs).

SiC MOSFETs have a theoretical performance figure-of-merit about 400x higher than silicon, but to date they have not reached their full potential. The relevant figure-of-merit is the quantity ($V_B^2/R_{ON,SP}$), where V_B is the blocking voltage and $R_{ON,SP}$ is the specific on-resistance (in Ω cm^2). The blocking voltage is typically limited by avalanche breakdown at the periphery of the device, while the on-resistance is limited by the channel resistance of the MOSFET. The blocking voltage *yield* is related to the density of material defects, most notably micropipes, while the on-resistance is determined by inversion layer electron mobility (at least in devices with drift regions less than 50 μm thick). The inversion layer mobility is dominated by an exponentially-increasing density of interface states in the upper half of the bandgap, particularly in 4H-SiC. These interface states are thought to arise from defects in the interfacial sub-oxide layer, a mix of Si-Si bonds, C-C bonds, and dangling bonds. The density of defects can be reduced by about one order-of-magnitude by a post-oxidation anneal in nitric oxide (NO). This results in the incorporation of nitrogen atoms at a density of about 10^{14} cm^{-2} within the interfacial sub-oxide, passivating many of the defects. Recent experiments also suggest that a subsequent post-oxidation anneal in H_2 in the presence of a Pt gate electrode can reduce the interface defect density by another factor of two. Measurements on test MOSFETs confirm a 5-10x increase in inversion layer mobility following the NO anneal, and results for the H_2 anneal are pending.

SiC BJTs are attractive because they do not depend upon a critical oxide, as do MOSFETs, and therefore are capable of operation at much higher temperatures. They are also immune to thermal runaway, a phenomenon that has limited the usefulness of BJTs in silicon. The primary disadvantage of BJTs relative to MOSFETs is the fact that they require large input drive current, complicating circuit design. To minimize the drive current, it is desirable to have a high common-emitter current gain β. We have found that β is limited by recombination in the neutral base at defects associated with lattice damage caused by the P+ base contact implant. By increasing the spacing between the emitter edge and the base contact, we have achieved $\beta > 50$, a record value for SiC BJTs. Further increases in β appear to be limited by carrier lifetime in the base under the emitter junction, and this too may be related to material or processing defects.

A final problem associated with ion implantation is a degradation in surface morphology during activation annealing due to step bunching and loss of silicon from the surface. This morphological degeneration can have serious implications for inversion mobility in DMOSFETs, where the inversion channel is formed on an implanted p-well. We have found that surface degradation can be mitigated by annealing in silane, and this will be discussed in the presentation.

NOTES

Process-dependent Device Characteristics of GaN-Based HEMTs

K. S. Boutros, M. Regan, P. Rowell, and B. Brar, (Rockwell Scientific)

Process control and reproducibility are critical for the maturation of GaN HEMT technology. Batch processing in epitaxial growth as well as device fabrication is a key enabler to quantify, correlate, and improve process parameters. This will lead to the identification and understanding of important process variables, and ultimately to improved control and reproducibility of the process.

To this end, we have performed preliminary work on process control through monitoring and mapping of material and device parameters of multiple wafer batches as a function of epitaxial growth runs and device fabrication lots. Multiple wafers from the same epitaxial run are used in the study. We have also investigated the effect of process change on wafers from the same growth batch and with similar epitaxial layer structure. Material and device parameters are mapped across the 2" wafers and correlation plots are generated to identify the wafer-to-wafer variation trends, as well as the sensitivity of the various device parameters to process related effects. The results of this study will be presented.

NOTES

Passivation Effects on PCM/DC/RF Performance of AlGaN/GaN HEMTs

R. C. Fitch *, N. A. Moser, G. H. Jessen, G. D. Via, J. K. Gillespie, A. Crespo
Air Force Research Laboratory, Sensors Directorate, 2241 Avionics Circle, WPAFB, Ohio 45433-7322

B. Lou and F. Ren
Department of Chemical Engineering, University of Florida, Gainesville, FL 32611, USA

B. P. Gila, C. R. Abernathy, S. J. Pearton
Department of Materials Science and Engineering, University of Florida, Gainesville, FL 32611, USA

* Corresponding author. Tel.: +1-937-255-1874 3453; Fax: +1-937-255-8656.
Email address: Robert.Fitch@wpafb.af.mil

Surface passivation of AlGaN/GaN High Electron Mobility Transistors has proven an effective means of reducing RF-dispersion and microwave power degradation. Materials such as silicon dioxide, silicon nitride, magnesium oxide, scandium oxide, and strontium fluoride have been evaluated for their ability to modify surface states and thus enhance device performance.[1,2] However, often the effects of these passivation schemes on the extrinsic device region are overlooked. In many cases, when the passivation is left to remain over the etched GaN buffer, serious pad-to-pad or inter-device leakage currents can arise. It is the nature and adverse affects of this leakage current that this work addresses. Standard AlGaN/GaN HEMT epi from eight epi vendors was processed using a baseline process which included a 1000Å deep chlorine-based inductively coupled plasma mesa etch, TiAlNiAu ohmic contacts, NiAu Schottky contacts, and plasma enhanced chemical vapor deposition silicon nitride passivation. The epi structure was consistently a top AlGaN layer with aluminum concentration between 25 and 35% and thickness between 200 and 300 Å. The GaN buffer beneath the AlGaN ranged from 1 to 2 microns in thickness. Some wafers were grown on SiC and others on sapphire. With nearly all of the epi processed, when inter-device isolation was compared before and after silicon nitride passivation, the leakage between isolated devices increased. In only two cases did the leakage remain in the nA range, and this was for material from the same vendor grown at the same time. Other wafers from this same vendor exhibited higher leakage currents. In all other wafers, the leakage increased from ten's of nA to as much as hundred's of uA. The mechanism for this increased leakage is being investigated and may be related to a combination of un-passivated surface states, intrinsic bulk buffer leakage and charge due to piezoelectric polarization at the GaN/SiN_x interface. DC, RF and process control monitor (PCM) performance for these devices will be reviewed.

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The Effects of Processing on Point Defects in AlGaN/GaN HEMTs with Correlation to Device Performance

G. H. Jessen,[a,*] G. D. Via,[a] J. K. Gillespie,[a] R. C. Fitch [a], B. D. White,[b] S. T. Bradley,[b] D. E. Walker,[b] L. J. Brillson[b]

[a] Air Force Research Laboratory, Sensors Directorate, 2241 Avionics Circle, WPAFB, Ohio 45433-7322

[b] Department of Electrical Engineering, The Ohio State University, 205 Dreese Laboratory, 2015 Neil Ave., Columbus, Ohio 43210

[*] Corresponding author. Tel.: +1-937-255-1874 x3384; fax: +1-937-255-8656.
Email address: Gregg.Jessen@wpafb.af.mil

Recent work has shown that optical defect emission spectra in AlGaN/GaN HEMTs can be correlated to device performance properties such as sheet resistance, contact resistance, and frequency response.[1,2] In this work, we use depth-dependent, spatially-localized, cathodoluminescence spectroscopy to correlate changes in specific point defect emissions with device fabrication procedures and ultimately, device performance. In this study of AlGaN/GaN HEMTs with Al mole fraction from 0.24 – 0.30 on silicon carbide and sapphire substrates, we observe the effects of reactive ion etching on the surface of the sample through changes in the AlGaN near band edge emission. We discern the highest concentration of specific point defects in GaN at the AlGaN/GaN interface and show that ohmic contact anneals at 850 °C reduce the point defects and affect interface quality. Furthermore, we spatially map the defect emissions and distinguish between the donor-acceptor pair (DAP) transitions and yellow-luminescence (YL) related transitions. Maps of the defect emission prior to annealing show a constant GaN DAP/YL emission ratio and show large variations after the ohmic contact anneal. We show that these defects interact to affect contact resistance and ultimately unity current gain frequency response. The DAP luminescence at 3.28 eV is associated with transitions from shallow donors to shallow acceptors such as Si, C, and Mg substitutional impurities. The YL at 2.25 eV is associated with transitions from shallow donors to deep level acceptors such as gallium vacancies and associated complexes with oxygen and hydrogen. Since these defects change as a function of device fabrication and have been shown to correlate with device performance, more materials characterization work is needed to understand the mechanisms of and control the introduction of these point defects during growth. These process improvements will ultimately lead to higher quality, more uniform devices.

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NOTES

Trap Engineering for Suppression of Current Collapse in AlInGaN-based Field Effect Transistors

Remis Gaska,[1] A. Khan,[2] M. S. Shur [3]

[1]*Sensor Electronic Technology, Inc., Columbia, SC 29209*

[2]*University of South Carolina, Columbia, SC 29208*

[3]*Rensselaer Polytechnic Institute, Troy, NY 12180*

In spite of the impressive results achieved for AlGaN/GaN Heterostructure Field Effect Transistors, conventional AlGaN/GaN heterojunction epilayer design has several limitations. The carrier confinement between the buffer and the active layer in this design is only due to the self-consistent triangular potential quantum well at the interface, and carriers can easily spill over into the buffer GaN or the barrier AlGaN layers, especially at a high drain bias. The spilled over carriers get trapped and thus give rise to slow transient processes and to the famous RF-current collapse. In addition, this spillover increases low frequency noise, decreases the device transconductance and breakdown voltage.

We developed and studied different device designs, which allowed us to identify which layer (GaN buffer layers, AlGaN barriers or AlGaN/GaN heterointerfaces) responsible for electron trapping causing the current collapse. These designs included GaN Doped Channel MESFETs (DC-MESFETs), AlGaN/GaN HFETs, AlGaN/InGaN/GaN Double HFETs and novel AlGaN/AlInGaN/InGaN/GaN Triple HFETs (THFETs).

Comparative studies of DC-MESFETs (that have no AlGaN barriers and AlGaN-GaN heterointerfaces) with different channel doping and AlGaN/GaN HFETs with various Al-content in AlGaN barrier (different band offset) showed that as much as 65-70% contribution to current collapse at RF frequencies comes from the GaN buffer layer. Having InGaN channel in AlGaN/InGaN/GaN DHFET design helped confine two-dimensional (2D) electrons close to AlGaN/InGaN heterointerface and prevent them from spilling over to GaN, which dramatically reduced the RF current collapse.

We also studied carrier dynamics in the buffer GaN layer using photoluminescence, time-resolved photoluminescence and light-induced transient gratings technique. We will present our preliminary data on the correlation between nonequilibrium carrier life-time, deep-level emission and current dispersion in AlInGaN-based transistors that elucidate the role of traps in current collapse.

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Bias-stress-induced current collapse in AlGaN/GaN HEMTs

S.C. Binari, J.A. Mittereder, P.B. Klein, D.S. Katzer, D.F. Storm, and J.A. Roussos
Naval Research Laboratory, Washington D. C. 20375

We have observed that current collapse can be induced in AlGaN/GaN HEMT structures as a result of short-term bias stress. This effect may be a contributing factor to the power output degradation observed in these devices and represents a potential reliability issue. The induced collapse appears to be permanent and can be reversed by SiN passivation, presumably through the formation of deep defect-H complexes. The traps responsible for the collapse have been studied by photoionization spectroscopy. This effect is attributed to hot carrier effects during stress.

NOTES

Aging and Degradation of AlGaN/GaN HFET's

T.J. Jenkins, R.C. Fitch, N.A. Moser, A. Crespo, J.G. Gillespie, G.H. Jessen, G.D. Via, M.J. Yannuzzi
Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH

Recent results of experiments involving aging and degradation of AlGaN/GaN HFET's will be discussed. The aging experiments involved unbiased transistors and process control monitors (PCM's), which were stored at elevated temperatures (150°C, 250°C, and 350°C). The degradation studies involved electrically stressing transistors (DC and RF conditions). The electrical stressing was completed on-wafer at room temperature and at elevated temperature. The key electrical characteristics of the transistors and process control monitors were periodically monitored to detect variations in performance. Significant changes in the transistors' and PCMs' characteristics were observed in the aging experiment. For example, sheet resistance increased by 4.4% (from 407 Ω/sq to 425 Ω/sq) after 168 hours of storage at 250°C. Significant changes associated with the Schottky contacts were observed. The turn-on voltage decreased 50%, and the gate leakage increased from 0.05 mA/mm to 1.25 mA/mm at V_{GS} = -3V and V_{DS} = 10V after 168 hours at 350°C. The DC and RF degradation studies observed significant changes and wide variations of changes from sample-to-sample, such as >1 dB decrease in output power after 60 hours.

NOTES

Nano-polytypes (Extended Stacking Faults) Induced in Ultrapure Epitaxial Films of 4H SiC when Grown on Heavily n-type Doped Substrates

W.J.Choyke
Department of Physics and Astronomy
University of Pittsburgh
Pittsburgh,PA 15260,USA.

The discovery of the degradation of the characteristics of SiC diodes under extreme electrical stress has stimulated much interest in the formation of stacking faults in SiC. We shall discuss the observation of stacking faults in epitaxial films of ultra-pure 4H SiC grown in hotwall reactors on heavily n-type doped 4H SiC wafers. We employ low temperature photoluminescence (LTPL) and high resolution transmission electron microscopy (HTEM) as characterization techniques.

Some background will be given as to how we are able to separate the intrinsic excitons from bound excitons and other sharp line spectral features. We will then show that in the majority of the cases investigated by us the extended stacking faults may be recognized as nano-polytypes of SiC with gaps smaller than that of 4H SiC.

Since it is well known that in heavily doped substrates the cubic modification of SiC may be induced by oxidation or thermal stress [1] we shall give some detailed high resolution results of cubic nano-polytype inclusions in ultra-pure epitaxial films grown on heavily doped substrates.

Our plans to use this technique for a "high-fidelity" study of the occurrence of stacking faults in substrates which have been oxidized or thermally stressed will be suggested.

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NOTES

Processing-Induced Generation of Stacking Faults in 4H-SiC

Ming Zhang[1], H. M. Hobgood[2], M.Treu[3], and P. Pirouz[1]
1. Department of Materials Science and Engineering, Case Western Reserve University, Cleveland, OH 44106-7204, USA
Tel: (216)-368-6496; FAX: (216)-368-3209; e-mail: pxp7@cwru.edu
2. Cree, Inc., 4600 Silicon Drive, Durham, NC 27703, USA
3. Infineon Technologies AG, Siemensstr. 2, A-9500 Villach, Austria

During high temperature device processing of 4H-SiC wafers heavily doped with nitrogen, visible signs of severe deformation were observed in certain regions of the wafers. The deformation was not uniform throughout but was localized in certain regions; most of the wafer did not show any visible change after processing. In addition, SIMS measurements showed a non-uniform nitrogen doping gradient across the wafer with the affected regions of the wafer having a higher nitrogen concentration than the non-affected regions. In this paper, a conventional and high-resolution transmission electron microscopy (TEM) examination of the microstructures of the affected and non-affected regions of a wafer having undergone this particular processing route is reported. While no defects were observed by TEM from the thin foils prepared from the non-affected region, a high density of stacking faults was observed in specimens made from the affected region. An examination of a few of the defects by HRTEM showed them all to be double-layer stacking faults that may have formed by the glide of Shockley partial dislocations on neighboring basal planes. The results are discussed in terms of the mechanism proposed by Lambrecht *et al.* (2001) on the stability of a faulted 4-SiC when the Fermi energy of the semiconductor is higher than the energy kevel of the stacking fault. We think that in the affected regions of the wafer, the n-doping had pushed the Fermi level to a value very close to the bottom of the conduction band.

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Thermoplastic Deformation and Stacking Faults in 4H- and 6H-SiC

Robert S. Okojie

NASA Glenn Research Center, 21000 Brookpark Road, Cleveland, OH 44135, USA
Ph. (216)433-6522; Fax (216)433-8643; E-mail: Robert.S.Okojie@nasa.gov.

Optical reflectometry was used to measure stress relaxation via thermoplastic deformation in as received 4H- and 6H-SiC substrates. In all cases, during thermal excursion to 500 °C, the radii of curvature of the substrates increased (i.e., became flatter) exponentially starting from ~350 °C. This change in curvature corresponded to a relaxation of the residual stress in the substrates. Upon cooling down to room temperature, the radii of curvature of all the substrates retained their high-temperature (500°C) values, thus exhibiting thermoplastic inelastic behavior. Further cyclic excursion to 500 °C did not yield any significant changes in the curvature, thus indicating that the changes from the first anneal were irreversible. The internal stress following thermoplastic deformation was estimated to be between 0.7 and 1 GPa at 500 °C. We also observed a significant difference in the thermoplastic deformation between the off- and on-axis substrates, with the latter having less change in the radius of curvature (ΔR = ~1 m) than the off-axis variation (ΔR > 3 m) at 500 °C. This difference suggests that the internal stresses in the off-axis 4H- and 6H-SiC substrates are inherently higher than corresponding on-axis SiC substrates. An on-axis n-type 6H-SiC that was subjected to thermal cycling between 150 °C and 900 °C in vacuum also exhibited thermoplastic deformation behavior, with activation energy of deformation of 3.14 ± 0.8 eV.

Subsequent measurements of residual stresses were performed on n-type 4H-SiC epilayers with different nitrogen-doping levels, grown homoepitaxially on the same n-type 4H-SiC substrates (ρ=0.01-0.011 Ω-cm) relaxed by thermal anneal in nitrogen at 1150 °C prior to growth. Stress measurements on the as grown epilayer on the substrate indicated the existence of a compressive stress in the epilayers. The samples were further annealed at 1150°C in nitrogen for thirty minutes and their microstructure was investigated by transmission electron microscopy (TEM), specifically to look for the possible generation of stacking faults (SFs). TEM investigations revealed 3C-SiC bands in the annealed 4H-SiC sample, some with with n-type epilayer doping as low as 5×10^{17} cm^{-3}. This epilayer doping level is approximately two orders of magnitude below the reported threshold value (3×10^{19} cm^{-3}) previously suggested for the onset of the generation of SFs in annealed epilayers [1]. This work provides evidence for the existence of significant compressive stresses in 4H-SiC epilayers. Thus, it is possible that stacking faults and 3C bands observed in many recent experiments are due to the motion of pre-existing partial dislocations.

Reference

[1] Thomas A. Kuhr *et al*, "Spontaneous formation of stacking faults in highly doped 4H-SiC during annealing", Journal of Applied Physics, **92**(10), 5863-5871. (2002).

NOTES

Processing-Induced Polytype Transformation in 4H-SiC

B.J. Skromme[1], M.K. Mikhov[1], L. Chen[1], H. Meidia[2], S. Mahajan[2],
Y. Ding[3], K.-B. Park[3], and J.P. Pelz[3]
[1]Department of Electrical Engineering and Center for Solid State Electronics Research
Arizona State University, Tempe, AZ 85287-5706
[2]Department of Chemical and Materials Engineering and Center for Solid State Electronics
Research, Arizona State University, Tempe, AZ, 85287-6006
[3] Department of Physics, The Ohio State University, Columbus, OH 43210-1106

Double stacking faults (3C inclusions) are spontaneously formed in heavily-doped n^+ 4H-SiC substrates during oxidation, thermal annealing, or as we show here, during epitaxy. Some of them propagate into overlying epilayers as well, leading to marked changes in the electrical properties of Schottky diodes formed on these layers. We will discuss our most recent progress in characterizing these faults and their properties, using high resolution transmission electron microscopy, low and room temperature photoluminescence (PL), and electrical (current-voltage, *I-V*, and capacitance-voltage, *C-V*) measurements on Schottky diodes. The current-voltage measurements can be modeled by a parallel diode model, in which virtually all the current flows through the lower barrier height regions where the cubic inclusions intersect the surface. The degree of Fermi level pinning is unaffected by the polytype transformation. In the present case, there is *no* lateral potential pinch-off effect, unlike the case of barrier height variations due to local changes in metal work function or interface states. The apparent lowering of barrier heights observed in the *C-V* measurements is explained by the charge in undepleted portions of the 3C inclusions within the depletion region. The 3C layers in the basal planes intersect the surface as straight lines, due to the 8° miscut of the wafers from the *c*-axis. These intersections are shown to be regions of locally lowered Schottky barrier height, using ballistic electron emission microscopy (BEEM) measurements performed at OSU. Measurements at ASU using secondary electron imaging (SEI) in a scanning electron microscope and also by electric force microscopy (EFM) show clear evidence of the local electric fields associated with these inclusions, which are believed to involve charge transfer (modulation doping) from the 4H matrix into the 3C wells. The SEI technique, in particular, is shown to be especially valuable as a rapid and very sensitive survey to detect these faults nondestructively, even in regions where they cannot by detected by room temperature PL. We observe spatial correlations in fault density with the local substrate doping level (observed by its optical transmission properties).

NOTES

Doping-Induced Stacking Faults in Hexagonal SiC Polytypes

M. Skowronski
Department of Materials Science and Engineering
Carnegie Mellon University

Structural and optical characteristics of doping-induced stacking faults have been investigated by electron microscopy, high resolution x-ray diffraction, and optical absorption techniques. In heavily n-type 4H-SiC (N_D>2x10^{19} cm^{-3}), faults are created by glide of two Shockley partial dislocations on two neighboring basal planes. This results in a band of six Si-C bilayers stacked in a cubic stacking sequence. Analysis of the Burgers vectors of bounding partial dislocations located at the interface of n^+ epilayers deposited on n-type substrates eliminated possibility of stress driving the fault expansion. Instead, the structural transformation is caused by lowering of the Fermi level position when electrons enter the quantum-well-like states associated with stacking faults. The free carrier absorption spectra indicate transfer of electrons to stacking faults and formation of depletion regions around them.

NOTES

Affect of oxidation and annealing on the defect levels in high purity semi-insulating 4H SiC

M.E. Zvanut and V.V. Konovalov, Dept of Physics, University of Alabama at Birmingham
W.C. Mitchel and W.D. Mitchell, Air Force Materials Laboratory, WPAFB, OH, 45433

Semi-insulating (SI) SiC may now be produced by a physical vapor transport process in which as yet unidentified intrinsic defects are used to compensate the unintentionally incorporated donors and acceptors. The material is referred to as HPSI SiC. Although temperature-dependent Hall resistivity measurements of these same wafers demonstrate that HPSI SiC is highly resistive, carrier activation energies (E_a) range between 1.1 and 1.5 eV throughout one wafer. We are studying the effects of oxidization and annealing on E_a and using electron paramagnetic resonance (EPR) spectroscopy to investigate the physical mechanisms responsible for the variations. EPR has an advantage over electrical characterization in that the samples need no contacts, so post-growth processing effects may be compared to as-grown material.

Although the defects observed by conventional EPR in HPSI SiC are most likely not those directly related to compensation, the work discussed below demonstrates that monitoring the 'dark' and photo-induced EPR spectra after oxidation and annealing provides valuable insight into potential processing affects. The 'dark' EPR spectra of HPSI SiC, which reflects the uncompensated carbon vacancies (V_C), is unaffected by a 1100 °C oxidization process similar to that used for MOS fabrication. However, the optical threshold energy (E_{th}) for the decay of V_C is changed by the oxidation. While a sharp threshold at 1.5 eV is observed in the as-grown material, a gradual decay beginning at photon energy as low as 0.5 eV occurs after oxidation. It is speculated that the decrease of V_C at photon energy greater than 0.5 eV is caused by the same defect or defects responsible for the variations in E_a observed among different pieces of the same wafer. This notion is further supported by the similarity between E_{th} measured in as-grown samples and E_a extracted from Hall measurements, both ranging between 1.1 and 1.5 eV. On a more practical note, the results suggest that parameters extracted from as-grown bulk SiC may not be appropriate for MOS devices.

Unlike oxidation, annealing as-grown HPSI SiC in an inert environment at temperatures above 1200 °C significantly changes the 'dark' EPR spectra. For example, 1600 °C annealing in pure Ar eliminates the carbon vacancy signal and produces an approximately equal concentration of shallow boron acceptors. However, temperature dependent Hall measurements performed on several pieces cut from the same wafer generally exhibit changes in E_a by no more than 0.3 eV after the same heat treatment. The small number of defects monitored by EPR reflects what the electrical measurements are 'covering up': that the shallow boron acceptor can become an uncompensated defect after high temperature annealing. The presence of uncompensated boron has not be reconciled with the electrical measurements which suggest the material is still semi-insulating. EPR detection of the shallow boron acceptor in highly resistive material suggests regions of microscopic inhomongeneities dispersed throughout the sample.

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NOTES

Steven Binari
Naval Research Laboratory
Code 6852
Washington, DC 20375
USA
Phone: (202) 404-4616
Fax: (202) 767-0455
E-mail: binari@nrl.navy.mil

Katherine Bogart
Sandia National Laboratories
Org 1126, MS 0601
PO Box 5800
Albuquerque, NM 87185
USA
Phone: (505) 844-6323
Fax: (505) 844-3211
E-mail: khbogar@sandia.gov

Karim Boutros
Rockwell Scientific Center
Materials and Devices
1049 Camino Dos Rios
Thousand Oaks, CA 91360
USA
Phone: (805) 373-4104
Fax: (805) 373-4860
E-mail: kboutros@rwsc.com

Leonard Brillson
The Ohio State University
205 Dreese Laboratory
2015 Neil Avenue
Columbus, OH 43210
USA
Phone: (614) 292-8015
Fax: (614) 688-4688
E-mail: brillson.1@osu.edu

W.J. Choyke
University of Pittsburgh
Physics and Astronomy
Pittsburgh, PA 15260
USA
Phone: (412) 624-9251
Fax: (412) 624-1479
E-mail: choyke+@pitt.edu

James Cooper
Purdue University
School of Electrical and Computer Engineering
465 Northwestern Avenue
West Lafayette, IN 47907-2035
USA
Phone: (765) 494-3514
Fax: (765) 494-2706
E-mail: cooperj@ecn.purdue.edu

Robert Davis
North Carolina State University
Box 7907
Raleigh, NC 27695-7907
USA
Phone: (919) 515-3272
Fax: (919) 515-7724
E-mail: robert_davis@ncsu.edu

Alan Doolittle
Georgia Institute of Technology
School of Electrical Engineering
777 Atlantic Drive
Atlanta, GA 30332-0250
USA
Phone: (404) 894-9884
Fax: (404) 385-0343
E-mail: alan.doolittle@ece.gatech.edu

Zhaoqiang Fang
Wright State University
Semiconductor Research Center/Physics Dept.
3640 Colonel Glenn Highway
Dayton, OH 45435
USA
Phone: (937) 775-3525
Fax: (937) 775-2222
E-mail: zhaoqiang.fang@wright.edu

Leonard Feldman
Vanderbilt University
Physics and Astronomy
Stevenson Center
Nashville, TN 27235
USA
Phone: (615) 343-7273
Fax: (615) 343-1708
E-mail: Leonard.c.feldman@vanderbilt.edu

Paul Fini
University of California, Santa Barbara
Bldg. 503, Room 1355
Santa Barbara, CA 93106-5050
USA
Phone: 805/893-2573
Fax: 805/893-8170
E-mail: fini@engineering.ucsb.edu

Robert Fitch
AFLR/SNDD
Bldg. 620, Rm S2-W66
2241 Avionics Circle
Wright-Patterson AFB, OH 45433-7322
USA
Phone: (937) 255-1874 x 3453
Fax: (937) 255-2306
E-mail: robert.fitch@wpafb.af.mil

Remis Gaska
Sensor Electronic Technology, Inc.
1195 Atlas Road
Columbia, SC 29209
USA
Phone: (803) 647-9757
Fax: (803) 647-9770
E-mail: Gaska@s-et.com

David Gotthold
EMCORE
145 Belmont Drive
Somerset, NJ 08873
USA
Phone: (732) 271-9090, ext. 4279
Fax: (732) 271-9686
E-mail: David_Gotthold@emcore.com

Evelyn Hu
University of California at Santa Barbara
Department of Materials
Electrical and Computer Engineering
Santa Barbara, CA 93106-9560
USA
Phone: (805) 893-2368
Fax: (805) 893-8170
E-mail: hu@ece.ucsb.edu

Gregg Jessen
Air Force Research Laboratory
AFRL/SND, Building 620
2241 Avionics Circle
Wright-Patterson AFB, OH 45433-7322
USA
Phone: (937) 255-1874, ext. 3384
Fax: (937) 255-8656
E-mail: Gregg.Jessen@wpafb.af.mil

Dan Johnstone
Virginia Commonwealth University
Electrical Engineering
601 West Main Street
Richmond, VA 23284
USA
Phone: (804) 827-7000, ext. 357
Fax: (804) 828-4269
E-mail: DJohnstone@vcu.edu

Ken Jones
U.S. Army Research Laboratory
2800 Powder Mill Road
Adelphi, MD 20783-1197
USA
Phone: (301) 394-2005
Fax: (301) 394-4562
E-mail: kajones@arl.army.mil

Asif Khan
University of South Carolina
Room 3A79
Swearingen Buliding
Columbia, SC 29208
USA
Phone: (803) 777-7941
Fax: (803) 777-2447
E-mail: asif@engr.sc.edu

William Lampert
US Army Research Office
PO Box 12211
Research Triangle Park, NC 27709-2211
Phone: 919/549-4325
Fax: 919/549-4399
E-mail: lampertwv@aro.arl.army.mil

Umesh Mishra
University of California at Santa Barbara
Department of ECE
Room 5107
Santa Barbara, CA 93106
USA
Phone: (805) 893-8956
Fax: (805) 893-8714
E-mail: mishra@ece.ucsb.edu

William Mitchel
Air Force Research Laboratory
AFRL/MLPS
3005 Hobson Way, Room 243
Wright-Patterson AFB, OH 45433-7707
USA
Phone: (937) 255-4474, ext. 3214
Fax: (937) 255-4913
E-mail: william.mitchel@wpafb.af.mil

Suzanne Mohney
Penn State
Materials Science and Engineering
109 Steidle Building
University Park, PA 18602
USA
Phone: (814) 863-0744
Fax: (814) 865-2917
E-mail: mohney@ems.psu.edu

Robert Nemanich
North Carolina State University
Department of Physics
110 Cox Hall
Raleigh, NC 27695
USA
Phone: (919) 515-3225
Fax: (919) 515-7331
E-mail: robert_nemanich@ncsu.edu

Robert Okojie
NASA-Glenn Research Center
Sensors and Electronics Technology
21000 Brookpark Road
Cleveland, OH 44136
USA
Phone: (216) 433-6522
Fax: (216) 433-8643
E-mail: robert.okojie@grc.nasa.gov

Pirouz Pirouz
Case Western Reserve University
Dept. of Materials Science and Engineering
1900 Euclid Ave., 500 White Building
Cleveland, OH 44106-7204
USA
Phone: (216) 368-6486
Fax: (216) 368-6033
E-mail: pxp7@cwru.edu

Mulpuri Rao
George Mason University
Electrical and Computer Engineering
4400 University Drive, MSN:1G5
Fairfax, VA 22030-4444
USA
Phone: (703) 993-1612
Fax: (703) 993-1601
E-mail: rmulpuri@gmu.edu

Deepak Selvanathan
University of Illinois
319 Micro & Nanothechnology Laboratory
208 North Wright Street
Urbana, IL 61801
USA
Phone: (217) 333-4052
Fax: (217) 244-6375
E-mail: Selvanat@uiuc.edu

Marek Skowronski
Carnegie Mellon University
Department of Materials Science and Engineering
5000 Forbes Avenue
Pittsburgh, PA 15213
USA
Phone: (412) 268-2710
Fax: (412) 268-7596
E-mail: ms3s@andrew.cmu.edu

Brian Skromme
Arizona State University
Department of Electrical Engineering
Box 875706
Tempe, AZ 85287-5706
USA
Phone: (408) 965-8592
Fax: (408) 965-8118
E-mail: skromme@asu.edu

Ioulia Smortchkova
Northrop Grumman Space Technology
1 Space Park, R6/2134 A
Redondo Beach, CA 90278
USA
Phone: (310) 812-6254
Fax: (310) 812-4378
E-mail: ioulia.smorchkova@trw.com, ysmor@yahoo.com

Jim Speck
University of California at Santa Barbara
Materials Department
Santa Barbara, CA 93106
USA
Phone: (805) 893-8005
Fax: (805) 893-8983
E-mail: speck@mrl.ucsb.edu

Mike Spencer
Cornell University
Electrical and Computer Engineering
Rm 418, Phillips Hall
Ithaca, NY 14853
USA
Phone: (607) 255-6271
Fax: (607) 255-4742
E-mail: spencer@ee.cornell.edu

Todd Steiner
AFOSR/NE
Physics & Electronics Directorate
4015 Wilson Boulevard, Suite 713
Arlington, VA 22203
USA
Phone: (703) 696-7314
Fax: (703) 696-8481
E-mail: todd.steiner@afosr.af.mil

Gerald Witt
Air Force Office of Scientific Research
AFOSR/NE
4015 Wilson Blvd., Room 713
Arlington, VA 22203-1954
USA
Phone: (703) 696-8571
Fax: (703) 696-8481
E-mail: gerald.witt@afosr.af.mil

Scott Wolter
US Army Research Office
PO Box 12211
Research Triangle Park, NC 27709-2211
Phone: 919/549-4353
Fax: 919/549-4399
E-mail: scott.wolter@us.army.mil

Colin Wood
Office of Naval Research
Code 313
800 North Quincy Street
Arlington, VA 22217-5660
USA
Phone: (703) 696-4218
Fax: (703) 696-2611
E-mail: Woodc@onr.navy.mil

Ed Yu
University of California at San Diego
ECE Department
9500 Gilman Drive, MC0407
LaJolla, CA 92093-0407
USA
Phone: (858) 534-6619
Fax: (858) 822-3425
E-mail: ety@ece.ucsd.edu

Mary Ellen Zvanut
University of Alabama at Birmingham
Physics Department
1530 3rd Avenue South, CH 310
Birmingham, AL 35244-1170
USA
Phone: (205) 934-6661
Fax: (205) 934-8042
E-mail: zvanut@phy.uab.edu

Meeting Planning Services Provided by:
Shari Allwood
Allwood & Associates, Inc.
8279 Midland Road
Mentor, OH 44060
PH: 440/951-1380
Fax: 440/951-1381
E-mail: AllwoodInc@aol.com